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MORRISON & FOERSTER LLP
755 PAGE MILL RD
PALO ALTO, CA 94304-1018

EXAMINER

SILVER, DAVID

ART UNIT	PAPER NUMBER
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2128

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary

Application No.

10/713,729

Applicant(s)

MCGAUGHY ET AL.

Examiner

David Silver

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>1/25/07</u> . | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-24 were originally presented for examination.
2. Claims 1-24 were rejected.
3. Claims 1-24 are currently pending in Instant Application.
4. The Instant Application is not currently in condition for allowance.

Priority

5. Priority is not claimed.

Information Disclosure Statement

6. The information disclosure statement(s) (IDS) submitted on 1/25/2007 is/are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement(s) is/are being considered by the examiner if signed and initialed by the Examiner.

Response to Arguments

Response: Claim Objections

7. **Applicants argue:**

Claim Objections

Applicants have also amended claims 1, 5, 9, 13, 17, and 21 to remove the "if" statement. The support for the amended claims 1, 5, 9, 13, 17, and 21 is found in Figures 9B and 9C and their corresponding descriptions in paragraphs [0037] to [0039] from page 25 to 27 of the pending application.

(Remarks dated 1/25/2007 ("Remarks"): page 12)

8. **Examiner Response:**

Applicants have placed the above paragraph under section "Claim Objections"; however, the Previous Office Action did not present Claim Objections. Further, the word "also" appears to indicate that a portion above was omitted. This appears to be a minor oversight.

However, clarification is respectfully requested if a portion was indeed inadvertently omitted.

Response: 35 U.S.C. §101

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9. Background:

9.1 Claims 1-8, and 17-24 stand rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

10. Applicants argue:

10.1 "As one of ordinary skill in the art would recognize that "simulating the group of leaf circuit ..." as recited in Claims 1-8 and 17-24 generates predicted behavior of the circuit. Referring to Figures 1 and 3A of the present application, the simulation results (i.e., the predicted behavior) may be displayed for example, in the form of waveforms 128, on a computer screen for engineers to inspect.

10.2 "These simulation results may be used to detect and correct design errors and to optimize design parameters, for example. Thus, similarly to the process in State Street, "simulating the group of leaf circuit ..." as recited in Claims 1-8, and 17-24 is a practical application in the technological arts because it transforms data (e.g., a netlist description of the circuit) into a useful, concrete, and tangible result simulation results such as, for example, waveforms or measurements. In particular, these simulation results are useful, concrete, and tangible in the same sense as was the final share price (a calculated number) cited in State Street." (Remarks: page 13)

10.3 "In response, Applicants submit that claims 17-24 do explicitly include a medium for storing computer programs, which is the memory described in claim 17. In addition, claim 17 also requires that the simulator module (a computer program) is used in conjunction with at least a processing unit (CPU), a user interface, and a memory, all of which are shown in Figure 7 of the pending application." (Remarks: page 14 third paragraph)

11. Examiner Response:

11.1 Regarding subsections 1 and 2 *supra*, it is noted that the features upon which applicant relies (i.e., displaying of the results on a computer screen) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). As

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the claims stand, they merely performs calculations (simulates), which, *per se*, do not produce concrete, useful, and **tangible final results** (emphasis added). See MPEP 2106.C.2.(2).

11.2 Regarding subsection 3 *supra*, rejections have been withdrawn in view of Applicants' remarks.

Response: Double Patenting

12. Background:

12.1 Claims 1-24 stand rejected on the ground of nonstatutory double patenting over claims 1-18 of U. S. Patent No. 7,024,652.

13. Applicants argue:

13.1 "As recited in the pending claims, the port connectivity interface is a dynamically created data structure during simulation, which person skilled in the art would understand is different from the matrix of U.S. 7,024,652. The matrix is used for the purpose of computation, while the port connectivity interface is used for communicating changes in signal conditions among the group of leaf circuits." (Remarks: page 14)

13.2 "The claim of U.S. 7,024,652 examines the strength of coupling signals between two leaf circuits in order to determine the strength of couple between the two leaf circuits. On the other hand, **paragraphs [0037] to [0039] of the specification** describe the method for evaluating the isomorphic behavior of two leaf circuits. In particular, the method determines whether the two leaf circuits have 1) a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits; 2) a substantially same set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits; and 3) a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals. For at least the reasons presented above, Applicants submit that the double patenting rejection should be withdrawn." (Remarks: page 15; emphasis by Examiner)

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13.3 "It is known in the art that during a simulation, the simulator needs to keep track of port connectivity information of the circuit components." (Remarks: page 17 first full paragraph)

13.4 "It is also known that during a simulation, the circuit components will go through different dynamic states." (Remarks: page 17 first full paragraph)

14. **Examiner Response:**

14.1 Regarding subsection 1 *supra*, the matrix is a "set of equations that represent the one or more leaf circuits contained in the group circuit. The group circuit matrix also contains solution vectors corresponding to the set of equations." (**col: 9 line: 51-56**). Further, "[a] group circuit is associated with a group solver for solving the matrix associated with the group circuit. A group circuit also includes reference to an event, which supports adding and deleting circuits in the group **dynamically** in response to **changes in signal conditions during simulation.**" (**col: 14 line: 36-49**)

14.2 Applicant's attention is drawn to (**Fig 8A item 808; Fig 9B, 9C and their descriptions**) which disclose the claimed isomorphic partitioning.

14.3 Regarding subsection 2 *supra*, the Applicants are arguing features not claims in claim 1.

Response: 35 USC §112 first / second paragraph

15. **Background:**

15.1 Claims 2, 6, 10, 14, 18, and 22 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement.

15.2 Claims 9-16 were rejected under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential structural cooperative relationship of elements, such omission amounting to a gap between the necessary structural connections.

16. **Applicants argue:**

16.1 "In response, Applicants have amended claims 2, 6, 10, 14, 18, and 22 to replace the "observe by" language in these claims." (Remarks: page 15)

16.2 "In response, Applicants have amended claim 9 to include the limitation of a simulator module.

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Claims 10-16, which variously depend from claim 9, therefore also include this limitation of the simulator module. The support for the amended claim 9 is found in Figures 7 and its corresponding descriptions from page 18 to 20 of the pending application." (Remarks: page 15)

17. Examiner Response:

The above-cited rejections have been withdrawn in view of the Applicants' amendments.

18. Background:

18.1 Claims 2-3, 5-7, 10-11, 14, 17-19, and 21-23 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

19. Applicants argue:

19.1 "In response, Applicants have amended claims 2, 10, and 18 to clarify the meaning of "substantially same isomorphic behavior" and have amended claims 6, 14, and 22 to clarify the meaning of "substantially different isomorphic behavior."

19.2 In each of the claims 2, 6, 10, 14, 18, and 22, Applicants further define the meaning of "substantially same" in the context of electrical signals that are within a predetermined threshold of signal tolerance. In other words, a person skilled in the art would understand that in order to determine whether two signals are substantially the same, a predetermined threshold of signal tolerance is used. If the two signals are within the predetermined threshold of signal tolerance, they are deemed to be substantially the same. On the other hand, if the two signals have deviated such that they are not within the predetermined threshold of signal tolerance, they are deemed to be not substantially the same (or substantially different). In practice, a person skilled in the art would understand that the predetermined threshold of signal tolerance may be programmed by designers as simulation parameters prior to the actual simulation." (Remarks: page 16; emphasis by Examiner)

20. Examiner Response:

Applicants are thanked for clarifying their invention. The rejections have been withdrawn in view of

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the above-recited arguments and the emphasized portions.

Response: 35 USC 102(e) Rejection

21. Background:

21.1 Claims 1-24 stand rejected under 35 U.S.C. 102(e) as being anticipated by Tcherniaev (U.S. Patent No. 6,577,992).

22. Applicants argue:

22.1 Specifically, the Tcherniaev reference does not disclose at least the elements "representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior; creating a first port connectivity interface dynamically for the group of leaf circuits in response to the merged leaf circuit; wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits" of the pending independent claims. ("Remarks: bottom of page 16 to top of page 17; emphasis in original)

22.2 "Applicants submit that one of the key differences between the current invention and the Tcherniaev reference lies in how dynamic information among the circuit components under simulation is communicated and what data structure are used for communicating such dynamic information during a transient simulation." (Remarks: page 17)

22.3 "It is known in the art that during a simulation, the simulator needs to keep track of port connectivity information of the circuit components." (Remarks: page 17 first full paragraph)

22.4 "It is also known that during a simulation, the circuit components will go through different dynamic states." (Remarks: page 17 first full paragraph)

22.5 "In the Tcherniaev reference, it chose to store such information in the static database while the current invention uses a newly created dynamic data structure called the port connectivity interface for storing and communicating such dynamic information during simulation. [...] Therefore, the method of passing information through the hierarchies, as taught by Tcherniaev, and synchronizing

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at each intermediate level would result in lower simulation performance." (Remarks: page 17 second full paragraph; underlining emphasis in Original)

22.6 "It is clear that the Tcherniaev reference teaches storing dynamic simulation information in the static subcircuit storage and using pointers to traverse the hierarchical data structure for passing dynamic information among subcircuits under simulation. The Tcherniaev reference is totally silent about the design issues, such as multiple program calls and synchronization between hierarchies, associated with its approach. No dynamic data structure, such as the port connectivity interface, is created by the Tcherniaev reference in response to the isomorphic behavior of the group of leaf circuits under simulation. The present invention addresses these design issues by using the port connectivity interface to facilitate communication of dynamic information among circuit components under simulation." (Remarks: bottom half of page 28; underlining emphasis in Original)

23. **Examiner Response:**

Attention is drawn to **(col: 3 line: 56-67)**, which discloses dynamic data structures (holds the dynamic voltage states) used in conjunction with the static storage. Therefore, when taken as a whole, Tcherniaev indeed has a "dynamic data structure", which directly correlates to the port connectivity interface claimed in the Instant Application.

24. **Applicant argues:**

24.1 "With respect to claims 5, 13, and 21, Applicants respectfully submit that the Tcherniaev reference does not disclose at least the element "splitting the merged leaf circuits into two or more individual leaf circuits in response to the two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors; creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits; wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits."" (Remarks: page 19)

25. **Examiner Response:**

25.1 Applicants statement amounts to general allegation and conclusionary statements of

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patentability.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

26. Claims 1-8 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

MPEP 2106 recites, in part:

"...USPTO personnel shall review the claim to determine it produces a useful, tangible, and concrete result. In making this determination, the focus is not on whether the steps taken to achieve a particular result are useful, tangible, and concrete, but rather on whether the *final* result achieved by the claimed invention is "useful, tangible, and concrete."

26.1 The method claims do not produce a useful, tangible, and concrete final **result**. The steps of the method claims do not produce a useful, tangible, and concrete result. They merely recite a software algorithm, *per se*, which, for example, does not display, store, or otherwise provide a useful tangible output. Note exemplary claim 1 which only recites software steps and does not produce a useful tangible and concrete result. Although a simulation is claimed as the last limitations, there does not appear to be a final **result** formed by the simulation.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

27. Claims 1-24 are rejected on the ground of nonstatutory double patenting over claims 1-18 of **U. S.**

Patent No. 7,024,652 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the

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patent since the patent and the application are claiming common subject matter. The Previous Office Action (dated 9/25/06) provides for the mapping of the pending Application and the US Patent.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

28. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Tcherniaev (**US 6,577,992**).

Tcherniaev teaches: 1. A method of simulating a circuit having a hierarchical data structure, comprising:

representing the circuit as a hierarchically arranged set of branches, including a root branch and

a plurality of other branches logically organized in a graph (**Fig 2A and text further expanding on the features**);

the hierarchically arranged set of branches including a first branch that includes one or more leaf circuits and a second branch that includes one or more leaf circuits (**Fig 2A and text further expanding on the features**);

wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches (**Fig 2A and text further expanding on the features**);

selecting a group of leaf circuits from the first and second branches for simulation (**Fig 2A items 206 & 208 and text further expanding on the features**);

representing the two or more leaf circuits as a merged leaf circuit in response to two or more leaf circuits of the circuit having a substantially same isomorphic behavior (**col: 3 line: 56 to col: 4 line: 27**);

creating a first port connectivity interface dynamically for the group of leaf circuits in response to

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the merged leaf circuit (**col: 4 line: 44-47; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**);

wherein the first port connectivity interface communicates changes in signal conditions among the group of leaf circuits (**col: 4 line: 44-47; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**); and

simulating the group of leaf circuits in accordance with the first port connectivity interface (**col: 4 line: 44-47; col: 4 line: 53-59; Fig 2B; Fig 2C-2D; Fig 3 items 306 and 308; and text which further expands on the figures features**).

Tcherniaev teaches: 2. The method of claim 1, wherein the substantially same isomorphic behavior comprises:

a substantially same set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits (**Fig 4 and texts further expanding on the features**);

a substantially same set of internal topologies, internal states, and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits (**col: 3 line: 40-44; col: 3 line: 56 to col: 4 line: 27**); and

a substantially same set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to the substantially same set of input signals (**col: 3 line: 56 to col: 4 line: 27**).

Tcherniaev teaches: 3. The method of claim 1, wherein the substantially same isomorphic behavior is monitored at the output ports of the leaf circuits and at the first port connectivity interface of the group of leaf circuits (**col: 3 line: 56 to col: 4 line: 27**).

Tcherniaev teaches: 4. The method of claim 1, wherein the first port connectivity interface comprises:

a set of input vectors for referencing to a set of input ports of one or more receiver leaf circuits; a set of output vectors for referencing to a set of output ports of one or more driver leaf circuits; a set of load vectors for referencing to a set of loads of the one or more driver leaf circuits; and an array of storage elements for storing information associating the set of loads to the set of input ports (**Fig 2A,**

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Fig 2B, Fig 2D (item 260 Elements Connectivity Model Parameter / Fanin/Fanout list / Port connectivity), Fig 3 item 304, Fig 2E and texts which further expand on the figures features).

Tcherniaev teaches: 5. The method of claim 1, further comprising:

splitting the merged leaf circuits into two or more individual leaf circuits in response to two or more leaf circuits represented by the merged leaf circuit demonstrating substantially different isomorphic behaviors **(Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9 item**

818; Fig 10 item 1012; and texts which further expand on the figures features);

creating a second port connectivity interface dynamically for the selected group of leaf circuits in response to the two or more individual leaf circuits **(Fig 4 item 414; Fig 8 item 726; Fig 9**

item 818; Fig 10 item 1012; and texts which further expand on the figures features);

wherein the second port connectivity interface communicates changes in signal conditions among the group of leaf circuits **(Fig 4 item 414; Fig 8 item 726; Fig 9 item 818; Fig 10 item**

1012; and texts which further expand on the figures features); and

simulating the group of leaf circuits in accordance with the second port connectivity interface **(Fig 2A items 206 & 208 and text further expanding on the features).**

Tcherniaev teaches: 6. The method of claim 5, wherein substantially different isomorphic behaviors include one or more elements selected from the group consisting of:

a substantially different set of input signals within a predetermined threshold of signal tolerance are received by the two or more leaf circuits **(Fig 4 item 414; Fig 8 item 726; Fig 9 item 818; Fig 10 item 1012; and texts which further expand on the figures features and texts further expanding on the features);**

a substantially different set of internal topologies, internal states and external loads within a predetermined threshold of signal tolerance associated with the two or more leaf circuits **(Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9 item 818; Fig 10 item 1012; and texts which further expand on the figures features; col: 3 line: 40-44; col: 3 line: 56 to col: 4 line: 27);** and

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a substantially different set of output signals are produced within a predetermined threshold of signal tolerance by the two or more leaf circuits in response to a substantially same set of input signals (**Fig 4 item 410 "Coupling strength"; Fig 8 item 726; Fig 9 item 818; Fig 10 item 1012; and texts which further expand on the figures features; col: 3 line: 56 to col: 4 line: 27**).

Tcherniaev teaches: 7. The method of claim 5, wherein the substantially different isomorphic behaviors are monitored at the output ports of the leaf circuits and at the second port connectivity interface of the group (**col: 3 line: 56 to col: 4 line: 27**).

As per claim 8, note the rejection of claim 4 above. The Instant Claim is rejected under same prior-art teachings.

As per claims 9-14, note the rejection of claims 1-8 above. The Instant Claims are functionally equivalent to the above-rejected claims and therefore rejected under same prior-art teachings but for user interface (**col: 11 line: 57-59**), memory (**col: 26 line: 46-55**), netlist (**col: 3 line: 5-15**).

As per claims 17-24, note the rejection of claims 9-14 above. The Instant Claims are functionally equivalent to the above-rejected claims and therefore rejected under same prior-art teachings.

Conclusion

29. All claims are rejected.

30. The Instant Application is not currently in condition for allowance.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

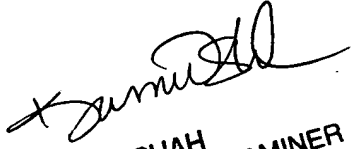
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date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Silver whose telephone number is (571) 272-8634. The examiner can normally be reached on Monday thru Friday, 10am to 6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Silver
Patent Examiner
Art Unit 2128


KAMINI SHAH
Supervisor
PATENT EXAMINER